

## Claims

- [c1] 1. A NAND flash memory cell row, comprising:
- a substrate;
  - a plurality of gate structures, disposed over the substrate, each of the gate structures comprising a tunneling dielectric layer, a floating gate, an inter-gate dielectric layer and a control gate;
  - a plurality of doped regions, disposed in the substrate between the gate structures, wherein the gate structures are connected in series;
  - a plurality of erase gates, disposed over the doped regions and between the gate structures;
  - a plurality of spacers, disposed between the gate structures and the erase gates;
  - a plurality of dielectric layers, disposed between the erase gates and the doped regions;
  - a first select gate and a second select gate, disposed on each of the sidewalls of two outermost gate structures respectively;
  - a plurality of select gate dielectric layers, disposed between the first select gate and the substrate and between the second select gate and the substrate;
  - a drain region, disposed in the substrate, wherein the

drain region is disposed on one side of the first select gate corresponding to the gate structures,; and a source region, disposed in the substrate, wherein the source region is disposed on one side of the second select gate corresponding to the gate structures.

- [c2] 2.The NAND flash memory cell row of claim 1, wherein the erase gate fills up spaces between the gate structures.
- [c3] 3.The NAND flash memory cell row of claim 1, wherein a thickness of the select gate dielectric layer is about 90 Å to 100 Å.
- [c4] 4.The NAND flash memory cell row of claim 1, wherein the inter-gate dielectric layer comprises silicon oxide/silicon nitride/silicon oxide composite layer.
- [c5] 5.The NAND flash memory cell row of claim 1, wherein the floating gate comprises polysilicon layer doped with arsenic.
- [c6] 6.The NAND flash memory cell row of claim 1, wherein a thickness of the dielectric layer is about 300 Å to 500 Å.
- [c7] 7.A NAND flash memory cell array, comprising:  
a plurality of memory cell rows, disposed two-dimensionally and arranged in a memory cell array,

wherein each of the memory cell rows comprises:

- a substrate;
- a plurality of gate structures, disposed over the substrate, wherein each of the gate structures comprises a tunneling dielectric layer, a floating gate, an inter-gate dielectric layer, and a control gate disposed on the substrate successively;
- a plurality of doped regions, disposed between the gate structures in the substrate, wherein the gate structures are connected in series;
- a plurality of erase gates, disposed over the doped regions and between the gate structures;
- a plurality of spacers, disposed between the gate structures and the erase gates;
- a plurality of dielectric layers, disposed between the erase gates and the doped regions;
- a first select gate and a second select gate, disposed on each of the sidewalls of the two outermost gate structures respectively;
- a plurality of select gate dielectric layers, disposed between the first select gate and the substrate, and the second select gate and the substrate;
- a drain region, disposed in the substrate, wherein the drain region is on one side of the first select gate corresponding to the gate structures; and
- a source region, disposed in the substrate, wherein the

source region is on one side of the second select gate corresponding to the gate structures ;  
a plurality of word lines, arranged in parallel along column direction, and each of the word lines is coupled to the control gates of the gate structures in a column;  
a plurality of bit lines, arranged in parallel along row direction, each of the bit lines is coupled to the drain region of the first select gate in a row;  
a source line, coupled to the source regions of the second select gates in the same column respectively; and  
a plurality of erase gate lines, arranged in parallel along column direction, and coupled to the erase gates in the same column.

- [c8] 8.The NAND flash memory cell array of claim 7, wherein the erase gate fills up spaces between the gate structures.
- [c9] 9.The NAND flash memory cell array of claim 7, wherein a thickness of the select gate dielectric layer is about 90 Å to 100 Å.
- [c10] 10.The NAND flash memory cell array of claim 7, wherein the inter-gate dielectric layer comprises silicon oxide/silicon nitride/silicon oxide composite layer.
- [c11] 11.The NAND flash memory cell array of claim 7, wherein

the floating gate comprises polysilicon layer doped with arsenic.

- [c12] 12.The NAND flash memory cell array of claim 7, wherein a thickness of the dielectric layer is about 300 Å to 500 Å.
- [c13] 13.A method of fabricating a NAND flash memory cell array, comprising:
  - providing a substrate;
  - forming a plurality of gate structures over the substrate, wherein the gate structures are formed in a row, and each of the gate structure comprises a tunneling dielectric layer, a floating gate, an inter-gate dielectric layer and a control gate sequentially disposed on the substrate;
  - forming a plurality of doped regions in the substrate between the gate structures;
  - forming a plurality of dielectric layers on the doped regions, and forming a plurality of first spacers on each of the sidewalls of the floating gates;
  - forming a plurality of erase gates between spaces of the gate structures;
  - forming a plurality of second spacers on each of the sidewalls of two outermost gate structures;
  - forming a plurality of first select gates and a plurality of second select gates on each of the sidewalls of the sec-

ond spacers;  
forming a drain region in the substrate, wherein the drain region is disposed on one side of the first select gates corresponding to the gate structures; and forming a source region in the substrate, wherein the source region is disposed on one side of the second select gates corresponding to the gate structures and the source region is coupled to a source line.

- [c14] 14.The method of claim 13, wherein the step of forming the gate structures comprises:  
forming a first dielectric layer over the substrate;  
forming a first conductive layer over the first dielectric layer;  
forming a second dielectric layer over the first conductive layer;  
forming a second conductive layer over the second dielectric layer;  
patterning the second conductive layer to form the control gate; and  
patterning the second dielectric layer, the first conductive layer, and the first dielectric layer, to form the gate dielectric layer, the floating gate and the tunneling dielectric layer.
- [c15] 15.The method of claim 14, wherein the method further comprises a step of forming a plurality of third spacers

on top and sidewalls of the control gates after the step of forming the control gates and before the step of forming the inter-gate dielectric layers, the floating gates and the tunneling dielectric layers.

- [c16] 16.The method of claim 1 5, wherein the method of forming the third spacers on top and sidewall of the control gates comprises a thermal oxidation.
- [c17] 17.The method of claim 1 5, wherein the step of forming the inter-gate dielectric layers, the floating gates and the tunneling dielectric layersuses the control gates and the third spacers as self-alignment masks.
- [c18] 18.The method of claim 13, wherein the step of forming the dielectric layer on the doped regions, and the step of forming the first spacers on sidewall of the floating gate comprise thermal oxidation.
- [c19] 19.The method of claim 13, wherein the step of forming the select gate dielectric layers over the substrate comprises thermal oxidation.
- [c20] 20.The method of claim 13, wherein the floating gate comprises polysilicon layer doped with arsenic.
- [c21] 21.A method operating of a NAND flash memory cell array, the memory cell array comprising a plurality of

memory cell rows, the memory cell in each of the memory rows being connected in series between a first select transistor and a second select transistor, each of the memory cells comprising a substrate, a tunneling dielectric layer, a floating gate, an inter-gate dielectric layer, a control gate, and a source/drain region, an erase gate being disposed between every two adjacent memory cells, a plurality of word lines being arranged in parallel along column direction and coupling to the control gates of the memory cells that are in same columns, a source line respectively coupling to source of the first select transistor in the same column, a plurality of bit lines respectively coupling to drain of the second select transistor, a first select gate line coupling to gate of the first select transistor that are in the same column, a second select gate line coupling to gate of the second select transistor of the same column, a plurality of erase gate lines being arranged in parallel along column direction and coupling to the erase gates in the same column, the operating method comprising:

for performing programming, zero voltage is applied to selected bit line, a first voltage is applied to non-selected bit line, a second voltage is applied to the first select gate line, a third voltage is applied to the word line of selected memory cell, a fourth voltage is applied to non-selected word line so as to program the selected

memory cell via Fowler-Nordheim tunneling effect; for performing read operation, a fifth voltage is applied to selected bit line, a sixth voltage is applied to the first select gate line, zero voltage is applied to the word line of selected memory cell, a seventh voltage is applied to non-selected word line so as to read the memory cell; and

for performing erase operation, an eighth voltage is applied to the erase gate line, a difference between the eighth voltage and voltage of the substrate is sufficient to remove electrons that are injected to the floating gate of the memory cell from the erase gateso as to erase the memory cell array.

- [c22] 22.The operating method of claim 21, wherein the first voltage is about 5 to 7 volts.
- [c23] 23.The operating method of claim 21, wherein the second voltage is about 10 to 20 volts.
- [c24] 24.The operating method of claim 21, wherein the third voltage is about 10 to 20 volts.
- [c25] 25.The operating method of claim 21, wherein the fourth voltage is about 5 to 7 volts.
- [c26] 26.The operating method of claim 21, wherein the fifth voltage is about 1 to 2 volts.

- [c27] 27.The operating method of claim 21, wherein the sixth voltage is about 5 to 7 volts.
- [c28] 28.The operating method of claim 21, wherein the seventh voltage is about 5 to 7 volts.
- [c29] 29.The operating method of claim 21, wherein the eighth voltage is about 10 to 20 volts.